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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PHAN, DEAN	
ART UNIT	PAPER NUMBER
2182	

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10/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,266	SCHMIDT, DOMINIK J.	
	Examiner	Art Unit	
	DEAN PHAN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20, 22-33, 35-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20,22-33 and 35-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05/20/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

- Applicant's amendment filed 06/16/2008 has been entered. Applicant has amended claims 20, 22, 33, 35 and 40, added claims 41, 42. Currently claims 20, 22-33, 35-42 are pending in this application. Any well known art statements made in the prior office action not argued by applicant is taken as admittance of prior art as per MPEP 2144.03.

Response to Arguments

Applicant's arguments filed on 06/16/2008 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

Prior art of record does not teach "non-reconfigurable host processor".

In response to argument, the Examiner respectfully traverses. In paragraph 14, the specification discloses "the host processor 148 is MIPS compatible". Note that "MIPS compatible" is not equivalent to "non-configurable". Nowhere in the specification discloses the host processor is non-configurable. Therefore the claims are rejected under 35 U.S.C. 112, first paragraph.

Additionally, in column 3 lns 50-55, Schmidt discloses "The reconfigurable processor core 150 can include one or more processors 151 such as MIPS processors..." Schmidt does not disclose said processor is a host processor. However, in the same field of art, APA discloses that it is known to provide processing systems having one or more central processing units, a memory and a host processor, such as the ARM processors or MIPS processors. The central processing units execute

dedicated code such as signal processing code, while the host processor coordinates the central processing units and interfaces with an external system (par. 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement a host processor in order to improve the performance and to take advantage of commercially available off the shelf system. (*see par. 2*).

Claim Objections

Claim 22 is objected to because of the following informalities: the claim 22 should be dependent on claim 20. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 20, 33, 40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter, *"non-reconfigurable host processor"*, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In paragraph 14, the specification discloses "the host processor 148 is MIPS compatible". Note that "MIPS compatible" is not equivalent to "non-configurable". Nowhere in the specification discloses the host processor is non-configurable.

Applicant is respectfully requested to indicate the portions of the specification which dictate the claimed subject matter. For the purpose of examination, Examiner treats the limitation as supported under the specification. Correction/Clarification is required.

Claims 20 and 40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, *"wherein the second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion to implement a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device*", which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In paragraph 14, the specification merely discloses "The number of active processors is controlled depending on the application". Nowhere in the specification discloses that the second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion to implement a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device. The rejection is similarly applied to claim 40. Applicant is respectfully requested to indicate the portions of the specification which dictate the claimed subject matter. For the purpose of examination, Examiner treats the limitation as supported under the specification. Correction/Clarification is required.

Claims 20, 33 and 40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. As to claim 20, the claim(s) contains subject matter, *"a processor type select circuit configured to select either the non-reconfigurable host processor or the second portion of the plurality of processors to implement the set of host processor functionality*", which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In paragraph 4, the specification merely discloses "a processor type select circuit to configure the integrated circuit to process instructions belonging to one of the first or second host processor family instruction set". Nowhere in the specification discloses that the processor type select circuit configured to select either the non-reconfigurable host processor or the second portion of the plurality of processors. The rejection is similarly applied to claim 33 and 40. Applicant is respectfully requested to indicate the portions of the specification which dictate the claimed subject matter. For the purpose of examination, Examiner treats the limitation as supported under the specification. Correction/Clarification is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20, 22-33, 35-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt (U.S 7142882) in view of Applicant Admitted Prior Art (hereafter APA).

As to claim 20, Schmidt a wireless communication device (Fig. 1) comprising: a single integrated circuit die (col 3 lns 38-45) including:

a reconfigurable processor core including a plurality of processors (fig. 1 Wireless COMM 100),

wherein a first portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a first processor family (*Either of CPU 151, ASIC 155, DSP 153 portions can be the first portion which is configured to execute instructions belonging to its family*) and

wherein a second portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a second processor family (*other portion that is not the first portion*),

wherein the second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion (DRAM FLASH 170) to implement a set of host processor functionality (col 3 lns 50-60) that includes controlling portions of the reconfigurable processor core (col 4 lns 1-39; “passed to the different functional elements”) and interfacing with a system external to the wireless communication device (col 4 ln 56 – col 5 ln 35);

a processor (*Any processor in the first portion*) coupled to the reconfigurable processor core (fig.1) and configured to execute instructions belonging to the instruction set of the first processor family *(For instance, the first portion CPU 151 which is configured to execute instructions belonging to its family)*, wherein the non-reconfigurable host processor is coupled to memory locations (fig. 1) storing instructions executable by the non-reconfigurable host processor to implement the set of host processor functionality (col 3 lns 55-67, col 4 lns 1-39).

a processor type select circuit configured to select either the non-reconfigurable host processor or the second portion of the plurality of processors to implement the set of host processor functionality (col 4 lns 25-33; "to produce various core control signals that are passed to the different functional elements of the processor core").

Schmidt does not disclose said processor is a host processor. However, in the same field of art, APA discloses that it is known to provide processing systems having one or more central processing units, a memory and a host processor, such as the ARM processors or MIPS processors. The central processing units execute dedicated code such as signal processing code, while the host processor coordinates the central processing units and interfaces with an external system (par. 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement a host processor in order to improve the performance and to take advantage of commercially available off the shelf system. (*see par. 2*).

As to claim 22, all limitations are in claim 20, wherein the first portion of the plurality of processors is configured to execute instructions corresponding to signal

processing functions (fig. 1 DSPs, col 3 lns 50-60) while the second portion of the plurality of processors executes the instructions stored in the memory locations that are executable to implement the set of host processor functionality.

As to claim 23, all limitations are in claim 20, further comprising a plurality of digital signal processors configured to execute instructions corresponding to one or more embedded signal processing functions (fig. 1 DSPs, col 3 lns 50-60).

As to claim 24, all limitations are in claim 20 but does not disclose the second portion of the plurality of processors collectively forms a second host processor. However, using two or more processors instead of a single one to handle and share a particular function is common in the art at the time of invention. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to collectively form the second portion of plurality of processors as a second host processor in order to avoid bottleneck problems, to improve the host performance and the stability of the device.

As to claim 25, all limitations are in claim 20, further comprising an analog circuit portion located on the integrated circuit (fig. 1 elements 110, 130, 111…) and coupled to a digital circuit portion (elements 150, 170, 190) that includes the host processor and the reconfigurable processor core, wherein the analog circuit portion includes:

a cellular radio core (element 110) configured to provide two-way communication via one or more wireless channels (col 4 ln 56-col 5 ln 20);

a radio sniffer coupled to the cellular radio core (element 111); and

a short-range wireless transceiver core coupled to the cellular radio core (element 130) and configured to provide two-way communication via one or more short-range wireless channels (col 5 lns 36-45).

As to claims 26-30, all limitations are in claim 25, wherein the reconfigurable processor core is coupled to the cellular radio core (fig. 1), and configured to process instructions corresponding to a plurality of wireless radio communication protocols includes a Bluetooth TM or IEEE802.11 protocol (col 4 ln 56-col 5 ln 2).

As to claim 31, all limitations are in claim 25, further comprising a router (elements 190) coupled to the host processor (col 1 lns 60-67), the cellular radio core (element 110), and the short-range wireless transceiver core (element 130), wherein the router is configured to track destinations of packets and to send the packets in a parallel through a plurality of separate wireless communication channels (col 6 lns 45-55).

As to claim 32, all limitations are in claim 31, wherein the router is further configured to determine which of the plurality of separate wireless communication channels provides an optimum transmission medium, and to send the packets in a parallel in response to determining that more than one or more channels is less than optimum (col 4 lns 40-55).

As to claims 33, 35-39, all same elements of Claims 20, 22-32 are listed, but in device form rather than method form. Therefore, the supporting rationale of the rejection to Claims 20, 22-32 applies equally as well to Claims 33, 35-39.

As to claim 40, all same limitations are in claim 20 with further: a system host processor (Fig. 2 CPU 220);

As to claims 41, all same limitations are in claim 20, wherein the second portion of the plurality of processors is further configured to execute instructions corresponding to signal processing functions (fig. 1 DSPs, col 3 lns 50-60) while the first portion of the plurality of processors executes instructions corresponding to signal processing functions.

As to claim 42, all same limitations are in claim 33, further comprising the second portion of the plurality of processors executing instructions corresponding to signal processing function (fig. 1 DSPs, col 3 lns 50-60) while the first portion of the plurality of processors executes instructions corresponding to signal processing functions.

Examiner's note:

Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEAN PHAN whose telephone number is (571)270-1002. The examiner can normally be reached on Mon - Thu; 9:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571) 272 6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dean Phan/
Examiner, Art Unit 2182
10/28/2008

/Tariq Hafiz/
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